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Our Case No. 9281-4673
Client Ref. No. S US02286

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Yasuhiko Ikarashi

Serial No. 10/736,924

Filing Date: 12/15/2003

For SIGNAL GENERATOR CAPABLE OF VARYING FREQUENCY OF AN OUTPUT SIGNAL OVER A WIDE RANGE

Examiner Michael B. Shingleton

Art Unit No. 2817

## AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of January 12, 2006. The Claims begin on page 2 and the Remarks begin on page 10.

**In the Claims:**

This listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1. (Previously presented) A signal generator, comprising:

a voltage controlled oscillation circuit;

a control voltage input terminal for inputting an external control voltage for determining a frequency of an oscillation signal;

a frequency divider circuit for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit;

a frequency divided signal output terminal for outputting a frequency divided signal output from the frequency divider circuit; and

a buffer amplifier which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the frequency divider circuit;

wherein the buffer amplifier has a balanced input and an unbalanced output.

Claims 2.- 4. (Canceled)

Claim 5. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillation circuit and the frequency divider circuit are arranged in an integrated circuit, and wherein the integrated circuit is provided with the control voltage input terminal and the frequency division signal output terminal.

Claim 6. (Original) The signal generator according to claim 5, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by a FET functioning as a voltage controlled variable capacitor.

Claim 7. (Original) The signal generator according to claim 5, wherein the

integrated circuit is formed utilizing CMOS technology.

Claim 8. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillation circuit employs field effect transistors (FET).

Claim 9. (Original) The signal generator of claim 6, wherein the voltage controlled oscillation circuit has a balanced output.

Claim 10. (Original) The signal generator according to claim 1, further comprising a circuit board on which the voltage controlled oscillation circuit and the frequency divider circuit are provided, wherein the control voltage input terminal and the frequency division signal output terminal are provided on end faces or an underside of the circuit board.

Claim 11. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillator circuit further comprises a varactor diode in a resonant circuit coupled to a base of an oscillating transistor.

Claim 12. (Original) The signal generator according to claim 11, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by the external voltage applied to the varactor diode.

Claim 13. (Original) The signal generator unit of claim 1, wherein a frequency division ratio of the frequency divider circuit is controlled by an externally applied switching signal.

Claim 14. (Original) The signal generator of claim 1, wherein a frequency division ratio of the frequency divided signal output is a whole number.

Claim 15. (Original) The signal generator of claim 1, wherein a frequency division ratio of the frequency divided signal output is a fractional number.

Claim 16. (Original) The signal generator of claim 1, further comprising a plurality of frequency divider circuits, one or more of the plurality of frequency divider circuits having a corresponding frequency divided signal output terminal.

Claim 17. (Original) The signal generator according to claim 16, wherein the frequency divided signal output from at least two of the plutality of frequency divider circuits are available simultaneously.

Claim 18. (Original) The signal generator according to claim 16, wherein the plurality of frequency divider circuits are connected in series.

Claim 19. (Original) The signal generator according to claim 16, wherein at least one of the plurality of frequency divider circuits is a variable frequency divider circuit capable of switching a frequency division ratio.

Claim 20. (Original) The signal generator according to claim 1, wherein the frequency divided signal output has a frequency that is equal to or lower than the frequency of the oscillation signal.

Claim 21. (Previously presented) A signal generator, comprising:

means for generating an oscillation signal;

means for frequency dividing the oscillation signal; and

means for outputting a frequency divided signal,

wherein a frequency of the oscillation signal is controlled by a first control means and a frequency division ratio of the frequency dividing means is controlled by a second control means; and

wherein the means for generating the oscillation signal comprises:

means for generating a balanced output oscillation signal;

means for converting the balanced output oscillation signal to an unbalanced output oscillation signal; and

means for inputting the unbalanced output oscillation signal to the means for frequency dividing the oscillation signal.

Claim 22. (Canceled)

Claim 23. (Original) The signal generator according to claim 21, wherein the means for frequency dividing the oscillation signal comprises:

means for cascading the means for frequency dividing,

wherein at least one of the cascaded means for frequency dividing is connected to the outputting means.

Claim 24. (Original) The signal generator according to claim 21, wherein the first control means is an externally applied control voltage.

Claim 25. (Original) The signal generator according to claim 21, wherein the second control means is an externally applied switching signal.

Claim 26. (Previously presented) A method of generating a signal with a wide frequency range, comprising:

generating a voltage controlled oscillation signal output;

frequency dividing the voltage controlled oscillation signal output;

controlling a frequency division ratio of the voltage controlled oscillation signal output; and

outputting a frequency divided signal;

wherein the generating a voltage controlled oscillation signal output comprising:

generating a balanced output oscillation signal;

converting the balanced output oscillation signal to an unbalanced output oscillation signal;

controlling a frequency of the balanced output oscillation signal.

Claim 27. (Canceled)

Claim 28. (Previously presented) The method according to claim 26, wherein controlling the balanced output oscillation signal comprises applying an external voltage.

Claim 29. (Original) The method according to claim 26, wherein controlling the frequency division ratio comprises applying an external switching voltage.

Claim 30. (Previously presented) A signal generator, comprising:

a voltage controlled oscillation circuit;

a control voltage input terminal for inputting an external control voltage for

determining a frequency of an oscillation signal;

a frequency divider circuit for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit;

a frequency divided signal output terminal for outputting a frequency divided signal output from the frequency divider circuit; and

a buffer amplifier which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the frequency divider circuit;

wherein the buffer amplifier is a common emitter transistor amplifier.

Claim 31. (Previously presented) The signal generator according to claim 30, wherein the voltage controlled oscillation circuit and the frequency divider circuit are arranged in an integrated circuit, and wherein the integrated circuit is provided with the control voltage input terminal and the frequency division signal output terminal.

Claim 32. (Previously presented) The signal generator according to claim 31, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by a FET functioning as a voltage controlled variable capacitor.

Claim 33. (Previously presented) The signal generator according to claim 31, wherein the integrated circuit is formed utilizing CMOS technology.

Claim 34. (Previously presented) The signal generator according to claim 30, wherein the voltage controlled oscillation circuit employs field effect transistors (FET).

Claim 35. (Previously presented) The signal generator of claim 32, wherein the voltage controlled oscillation circuit has a balanced output.

Claim 36. (Previously presented) The signal generator according to claim 30, further comprising a circuit board on which the voltage controlled oscillation circuit and the frequency divider circuit are provided, wherein the control voltage input terminal and the frequency division signal output terminal are provided on end faces or an underside of the circuit board.

Claim 37. (Previously presented) The signal generator according to claim 30, wherein the voltage controlled oscillator circuit further comprises a varactor diode in a resonant circuit coupled to a base of an oscillating transistor.

Claim 38. (Previously presented) The signal generator according to claim 37, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by the external voltage applied to the varactor diode.

Claim 39. (Previously presented) The signal generator unit of claim 30, wherein a frequency division ratio of the frequency divider circuit is controlled by an externally applied switching signal.

Claim 40. (Previously presented) The signal generator of claim 30, wherein a frequency division ratio of the frequency divided signal output is a whole number.

Claim 41. (Previously presented) The signal generator of claim 30, wherein a frequency division ratio of the frequency divided signal output is a fractional number.

Claim 42. (Previously presented) The signal generator of claim 30, further

comprising a plurality of frequency divider circuits, one or more of the plurality of frequency divider circuits having a corresponding frequency divided signal output terminal.

Claim 43. (Currently amended) The signal generator according to claim 42, wherein the frequency divided signal output from at least two of the ~~plutality~~ plurality of frequency divider circuits are available simultaneously.

Claim 44. (Previously presented) The signal generator according to claim 42, wherein the plurality of frequency divider circuits are connected in series.

Claim 45. (Previously presented) The signal generator according to claim 42, wherein at least one of the plurality of frequency divider circuits is a variable frequency divider circuit capable of switching a frequency division ratio.

Claim 46. (Previously presented) The signal generator according to claim 30, wherein the frequency divided signal output has a frequency that is equal to or lower than the frequency of the oscillation signal.

## REMARKS

### Summary

Claims 1, 5, 21, 23-26 and 28-46 are pending in the application and all of the claims were rejected in the present Office Action. Claim 43 has been amended. The Applicant has carefully considered the references and arguments presented by the Examiner, and respectfully traverses the rejections on the basis that a *prima facie* case of obviousness has not been made out.

The Applicant respectfully requests that this Office action be withdrawn and that a new Office action be issued which specifically addresses each of the claims in the application. The present Office action consists of a discussion of the references with reference to some but not all of the claims, and the record does not show whether a *prima facie* case of obviousness has been made out in the case of each and every claim of the present application.

This present Office action applies new art to previously allowable subject matter. In the previous Office action, the Examiner indicated that Claims 3, 4, 22, 27 and 28 were objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Claims 3 and 4 were cancelled, for example, and the subject matter of these claims was incorporated into Claim 1. It is accepted that such an amendment is not substantive, and should have placed the application in condition for allowance. Similar actions were taken with respect to the other objected to claims.

In the prosecution of an application, an applicant may have to consider the economic cost of continuing to argue claims that the applicant believes to be allowable, or the delay in patent issuance, and may, when the examiner offers allowance of some claims when rewritten as independent claims, choose to make such amendments, either abandoning the subject matter or continuing to prosecute the subject matter in a continuing application. In the present circumstances, the acquiesce of the applicant in having made claim amendments should therefore not be construed as having a material

bearing on the patentability of the subject matter not claimed, as the applicant is merely going forward from the position reached after responding to the previous Office action.

## Objections

Claim 43 was objected to on the basis of an informality. The claim has been amended to correct the typographical error, and the Applicant respectfully submits that the objection has been obviated.

## Claim Rejections

### 35U.S.C. §103 (a)

Claims 1, 5-12, 14, 20, 26 and 28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh (6,737,927; "Hsieh") in view of Segawa et al. (US 6,342,818)

Claim 1 reads, *inter alia,* a control voltage input terminal for inputting an external control voltage for determining a frequency of an oscillation signal, a buffer amplifier which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the variable frequency divider circuit, the variable frequency divider circuit for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit.

The Examiner characterizes Fig 1(a) of Hsieh as being the invention of the reference. However all of the discussion cited relates to statements made in the background section of the reference. As such, the reference may not be enabled. Without accepting that the reference is enabling for the subject matter cited, the Applicant nevertheless traverses the application of Hsieh

Hsieh teaches a frequency synthesizer of a closed-loop type where an output of a VCO is applied to a divide-by-N counter (17) in Fig. 1(a), and compared with a reference frequency $F_{ref}$ to form a feedback control signal to control the VCO so it is a multiple of $F_{ref}$. The frequency divider 16 as taught by Hsieh must be a fixed divide-by-two circuit as "[b]y dividing the frequency of the digital signal $F_{vco}$ by two, the duty cycle distortion can be disregarded." (col 1, line 66, bridging col. 2, line 1). Thus the output signal frequency of the device taught in the background section of Hseich is always half

of the VCO (14) output frequency and it can never be equal to the VCO output frequency. Without the divide-by N counter 17 in a feedback loop, the device taught by Hsieh will not function, as the control loop is not closed. In addition, the Examiner's contention that the divide-by-two circuit as in Hsieh could be configured for another dividing ratio (Office action, page 3, lines 10-16) would result in the device of Hseih being inoperative for its intended purpose (see Hseih, col. 1, line 60, bridging col 2, line 2). Certianly, Hsieh does not teach or suggest that another dividing ratio would be appropriate or effective at the position in the circuit taught by Hsieh, and any such suggestion must be considered impermissible hindsight. As such, the reference cannot be used as a teaching in an obviousness inquiry.

Since Hsieh is the primary reference, to be modified by any secondary references, and the primary reference is inoperative as characterized by the Examiner, the use of such a reference is not appropriate in making out a *prima facie* case. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). See *Tec Air Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999) (quoting *In re Sponnoble*, 405 F.2d 578, 587 (CCPA 1969)).

Moreover, Hsieh does not teach or suggest that there is a "control voltage input terminal for inputting an external control voltage". The Examiners characterization of an internal connection between the control-voltage generating device (10) and the VCO (14) as an input terminal is respectfully traversed. A fixed connection between devices integral to a circuit is not an input terminal for an external voltage. Here, and in many places in the Office action, the Examiner asserts that the references teach a "means" for doing something. This phrase now has a special meaning in view of the interpretation of 35 U.S.C. §112, ¶ 6, where the actual element being taught must be found in a reference. The Applicant respectfully requests that the Examiner provide an explanation as to how the term "means" is to be interpreted in the context of the Office action.

For at least the reasons given above, not all of the elements and limitations of Claim 1 are taught by the reference, a *prima facie* case has not been made out, and the claim is allowable.

Claims 5-12, 14, 20 26 and 28 are claims dependent on an allowable base claim and are allowable, without more.

Claims 13, 15, 21, 24, 25 and 29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh in view of Segawa as applied to Claims 1, 5-12, 14, 20, 26 and 28 above, and further in view of Berquist et al. (US 6,542,044; "Berquist").

Claim 21 is a means plus function claim and is entitled to be interpreted in accordance with MPEP 2182. The Examiner does not appear to have identified the elements in the references that are specifically used to teach the means that are recited in the specification of the present application. Therefore, a *prima facie* case of obviousness has not been made out. Claims 25 and 29, being claims dependent on an otherwise allowable claim are allowable, without more.

With respect to Claim 13, nothing in Berquist is cited to overcome the deficiencies in the rejection of Claim 1, and the claim is therefore not obvious, as well as being allowable, without more, as dependent on an allowable claim.

Claim 23 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh in view of Segawa and further in view of Berquist as applied to Claims 1, 5-15, 20, 21, 24-26, 28 and 29 above, and further in view of Vandergraaf (US 4.347,484; "Vandergraaf"). Claim 23 depends on claim 21. Should the Examiner intend to continue to reject this claim, the Applicants respectfully request that the specific aspects of the references being applied to Claim 21 and 23 be identified. As used in Hsieh, the Applicant has already asserted that a variable frequency divider is not an "art recognized equivalent" of a fixed frequency divider. Nothing in the arguments presented here by the Examiner is directed towards overcoming the deficiencies in the rejection of Claim 21, *supra*, and thus Claim 23 is not obvious. Claim 23 is also allowable as a claim dependent on an allowable claim, without more.

Claim 23 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh in view of Segawa as applied to Claims 1, 5-12, 14, 20, 21, 26, and 28 above, and further in view of Vandergraaf (US 4.347,484; "Vandergraaf"). The recitation of the reasons for rejection are essentially repetitive of those previously made and are respectfully traversed for the same reasons.

Claims 30-34, 36-42 and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berquist in view of Van Amesfoort (US 5,712,596; "Van Amesfoort") and Segawa.

Claim 30 recites, *inter alia*, a control voltage input terminal for inputting an external control voltage for determining a frequency of an oscillation signal.

The Examiner asserts that "the output terminal of the frequency divider is an internal terminal", but then appears to suggest that any of the connections made to a functional element of the block diagram may be considered as a terminal, and such terminals may be either internal or external terminals. In doing so, the Examiner cites MPEP 2111 as permitting the Examiner to take the broadest reasonable interpretation of the claims. [emphasis added]. However that does not extend to asserting a meaning of a claim limitation which is expressly disclaimed by the words themselves. The distinction between "internal" and "external" is unarguable, and the element of Claim 30 recited above is not found in any of the references cited by the Examiner. Thus, for at least this reason, a *prima facie* case of obviousness has not been made out, and Claim 30 is allowable.

In making rejections of Claims 31-34, 36-42 and 46, the Examiner has, as in the rejection of previous claims made a statement that a particular circuit or arrangement is an "art recognized" equivalent of an element or limitation of a claim. But no substantiation of this assertion is provided. These assertions are a form of "Official Notice" by another name, and the Applicant respectfully requests that in each instance where an "art recognized" equivalent is cited by the Examiner in any of the rejections made herein, that the Examiner provide either a suitable reference for that assertion or an affidavit giving the reasons that the Examiner has come to the conclusions stated.

Claims 31-34, 36-42 and 46, being claims dependent on an allowable claim are allowable, without more.

Claims 42-45 were rejected under 35 U.S.C. §103(a) as being unpatentable over Berquist in view of Van Amesfoort and Segawa as applied to Claims 30-34, 36-42 and 46 above, and further in view of Vandergraaf. The aspect of Vandergraff being asserted here is the same as that previously asserted by the Examiner and is traversed for the same reasons.

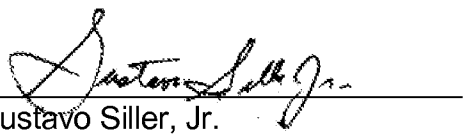
With respect to the rejections as a whole: "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 519 U.S. 822 (1996)(citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed.Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d1885, 1888 (Fed. Cir. 1991)).

The Applicants have traversed each and every claim rejection in sufficient detail to establish that the claim is allowable on the basis that at least one element of every claim is not obvious over the cited art. There are other aspects of the claims that constitute patentable subject matter, but it is only necessary to show that the claim is patentable, and not to traverse each and every one of the Examiner's reasons. The Applicant reserves the right to assert other traverses should the claims not be allowed.

## Conclusion

In view of the arguments above, Applicant respectfully submits that the pending claims are in condition for allowance and seek an early allowance thereof. If for any reason the Examiner is unable to allow the application in the next Office Action and believes that a telephone interview would be helpful to resolve any remaining issues, he is respectfully requested to contact the undersigned.

Respectfully submitted,



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